AMENDMENTS

LISTING OF CLAIMS:

1. **(Currently amended)** A self-refresh device, comprising:

a command decoder for outputting a mode register set signal, a self-refresh signal and a refresh flag signal by decoding an externally inputted refresh command;

a refresh counter for outputting a refresh request signal by performing a counting operation corresponding to a refresh cycle in response to the refresh flag signal;

an internal address counter for counting and generating an internal address in response to the refresh flag signal and the refresh request signal;

a partial array self-refresh decoder for ~~decoding and latching an address preset as an extended mode register set code in response to a mode register set signal, and then selectively activating~~ generating a plurality of control signals for performing a partial array self-refresh operation in response to the mode register set signal, the self-refresh signal, and the internal address ~~by combining corresponding addresses when a self-refresh signal is activated~~; and

a row address strobe generator for controlling a row active signal for selectively activating ~~at least~~ one or more banks or a certain region in a selected single bank depending on states of the plurality of control signals when a refresh operation signal is activated~~, or selectively activating a certain array region selected in a single bank~~.

2. **(Currently amended)** The device according to claim 1, further comprising:

~~a command decoder for outputting the mode register set signal, the self-refresh signal and a refresh flag signal by decoding an externally inputted refresh command;~~

~~a refresh counter for outputting a refresh request signal by performing a counting operation corresponding to a refresh cycle in response to the refresh flag signal;~~

~~an internal address counter for counting and generating an internal address in response to the refresh flag signal and the refresh request signal; and~~

a row pre-decoder for outputting an external address as a row address in a normal mode, and outputting the internal address as the row address in a refresh mode.

3-5. **(Canceled)**

6. **(Currently amended)** The device according to claim 1, wherein the partial array self-refresh decoder comprises:

an extended mode register set decoder for outputting a register set control signal by decoding a bank selection address in response to the mode register set signal;

a plurality of address latches each ~~of which~~ for outputting register set address bit by latching [[a]] an external address, in response to the register set control signal and the self-refresh signal when the mode register set signal is applied; and

a partial array self-refresh controller for selectively activating the plurality of control signals by decoding the plurality of register set addresses depending on ~~input of~~ the internal address.

7. **(Currently amended)** The device according to claim 6, wherein ~~the extended mode register set decoder activates~~ the register set control signal is activated when ~~at the activation of~~ the mode register set signal is activated, ~~when~~ a most significant bit address of the bank selection address is high, and a second most significant bit of the bank selection address is low.

8. **(Original)** The device according to claim 7, wherein the extended mode register set decoder comprises:

a first inverter for inverting the second most significant bit of the bank selection address;

a first NAND gate for NANDing the most significant bit of the bank selection address and an output signal of the first inverter;

a second inverter for inverting an output signal of the first NAND gate; and

a second NAND gate for outputting the register set control signal by NANDing the mode register set signal and an output signal of the second inverter.

9. **(Currently amended)** The device according to claim 6, wherein ~~on~~ each of the plurality of address latches comprises:

a first switch for selectively outputting one of the plurality of external addresses in response to the mode register set signal;

a first latch for latching an output signal of the first switch;

a second switch for selectively outputting an output signal of the first latch in response to the register set control signal;

a second latch for latching an output signal of the second switch; and

a first logic unit for outputting an output signal of the second latch as one of the plurality of register set addresses in activation of the self-refresh signal.

10. **(Original)** The device according to claim 9, wherein the first latch and the second latch, respectively, comprise a third inverter and a fourth inverter where each output signal is feedback as an input signal.

11. **(Original)** The device according to claim 9, wherein the first logic unit comprises:

a third NAND gate for NANDing the self-refresh signal and an output signal of the second latch; and

a seventh inverter for inverting an output signal of the third NAND gate.

12. **(Currently amended)** The device according to claim 6, wherein the partial array self-refresh controller outputs ~~first, second and third~~ the plurality of control signals ~~obtained~~ by decoding the plurality of register set addresses and the plurality of inverted register set addresses~~, and~~

~~the first control signal is selectively outputted in response to the internal address~~.

13. **(Currently amended)** The device according to claim 12, wherein one of the plurality of ~~the first~~ control signal is outputted ~~when a most and a second most significant bits of the internal address are both high, or~~ when at least one of the most and the second most significant bits of the bank selection address is high.

14. **(Currently amended)** The device according to claim 1, wherein the row address strobe generator ~~controls~~ generates the row active signal depending on a bank selection address and a normal operation signal ~~activated~~ in a normal mode, and generates ~~controls~~ the row active signal depending on the plurality of control signals and the refresh operation signal ~~activated~~ in a refresh mode.

15. **(Currently amended)** The device according to claim 14, wherein the row address strobe generator comprises:

a first switching means for being selectively turned on in response to the normal operation signal and the refresh operation signal;

a second switching means for being selectively turned on depending on ~~activation of~~ the bank selection address and ~~when~~ the normal operation signal ~~is activated, and then activating the row active signal~~; and

a third switching means for being selectively turned on depending on ~~activation of~~ the plurality of control signals and ~~when~~ the refresh operation signal ~~corresponding to a refresh request signal is activated, and then activating the row active signal~~.

16. **(Currently amended)** The device according to claim 15, wherein the first switching means comprises a first PMOS transistor and a second PMOS transistor connected in series between a power source terminal and the second switching means, wherein the first PMOS transistor and the second PMOS transistor having each gate to receive the normal operation signal and the refresh operation signal, respectively.

17. **(Currently amended)** The device according to claim 15, wherein the second switching means comprises a first NMOS transistor and a second NMOS transistor connected between the first switching means and a ground terminal, wherein the first NMOS transistor and the second NMOS transistor having gates to receive the normal operation signal and the bank selection address, respectively.

18. **(Currently amended)** The device according to claim 15, wherein the third switching means comprises a third NMOS transistor and a fourth NMOS transistor connected between the first switching means and a ground terminal, wherein the third NMOS transistor and the fourth NMOS transistor having gates to receive the refresh operation signal and the plurality of control signals.

19. **(Original)** The device according to claim 1, wherein the row address strobe generator is comprised to have the same number of the banks.

20. **(Canceled)**

21. **(New)** The device according to claim 6, wherein the extended mode register set decoder sets up a code for performing a self-refresh operation on a cell array corresponding to a half of one bank when a partial array self-refresh operation is in a half of bank mode, and for performing a self-refresh operation on a cell array corresponding to a quarter of one bank when a partial array self-refresh operation is in a quarter of bank mode.

22. **(New)** The device according to claim 21, wherein when the partial array self-refresh operation is in a half of bank mode, the partial array self-refresh decoder

activates a number of control signals corresponding to a quarter of the plurality of control signals until a most significant bit of address becomes high.

23. **(New)** The device according to claim 21, wherein when the partial array self-refresh operation is in a quarter of bank mode, the partial array self-refresh decoder activates a number of control signals corresponding to a quarter of the plurality of control signals until at least one of two most significant bits of address becomes high.